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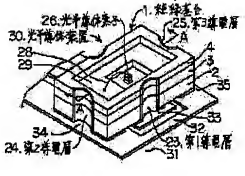
(54) OPTICAL SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To provide an optical semiconductor device which normally operates even if it is mounted on the reverse direction.
CONSTITUTION: A first conductive layer 23 residing in the central vicinity of the front surface of an insulating pedestal 1 and in the central vivinity of the reverse surface thereof is provided. Second and third conductive layers 24, 25 which are formed in the vicinity of at least an end part opposing to each other on the reverse surface of the insulating pedestal 1 and which are connected each other are provided. An optical semiconductor element 26 which is secured to in the central vicinity of the front surface of the first conductive layer 23 and which is wired to the second or third conductive layer 24, 25 is provided.



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CLAIMS

[Claim(s)]
[Claim 1]An optical semiconductor device comprising:
The 1st conductive layer provided by standing in a row near the center on the back near the center of the surface of an insulating base.
The 2nd and 3rd conductive lavers that were provided near [where a rear face faces at least]

the end of said insulating base, and were connected mutually.
An OPTO semiconductor device to which it adhered near the center of the surface of said 1st conductive layer and which was wired by said 2nd or 3rd conductive layer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the small optical semiconductor device by which chip making was carried out.
[0002]
[Description of the Prior Art]The optical semiconductor device which carried out small approximately core box shape by which chip making was carried out is proposed in recent years. This is shown by the sectional view of drawing 8 like JP,60-262476,A. The 1st and 2nd wiring layer 41 and 42 is located in the surface of the insulating base 43, and is extended and formed in the rear face through the side. The reflection frame 44 is laminated on the insulating base 43. And the light emitting diode 45 adheres on the 1st wiring layer 41, and is wired by the 2nd wiring layer 42.
[0003]
[Problem(s) to be Solved by the Invention]However, an optical semiconductor device like a lever adheres so that the reverse part of the 1st and 2nd wiring layer 41 and 42 may be located on the anode of the circuit board 46, the negative pole pattern 47, and 48, respectively, and forward voltage is impressed. so, an optical semiconductor device -- between ** -- when it attaches to an opposite direction (i.e., when the 1st and 2nd wiring layer 41 and 42 is adhered on the negative pole, the anode pattern 48, and 47), it becomes impossible (light is not emitted) of operation. Therefore, this invention cancels this fault, and even if it attaches to an opposite direction, it provides the optical semiconductor device which performs normal operation.
[0004]
[Means for Solving the Problem]This invention provides the 1st conductive layer formed by standing in a row near the center on the back near the center of the surface of an insulating base, in order to solve an above-mentioned technical problem. And it is formed near [where a rear face faces at least] the end of an insulating base, and the 2nd and 3rd conductive layers connected mutually are provided. An OPTO semiconductor device to which it furthermore adhered near the center of the surface of the 1st conductive layer and which was wired by the 2nd or 3rd conductive layer is formed.
[0005]
[Function]Since this invention forms the 1st conductive layer near the center of the rear face of an insulating base like ****, when this optical semiconductor device is attached for Masakata or to an opposite direction, the same polar voltage is impressed to the 1st conductive layer. And

the 2nd and 3rd conductive layers are connected, and it faces and forms near the end of the rear face of an insulating base. Therefore, when it attaches for Masakata or to an opposite direction, the same polar voltage is impressed to the 2nd or 3rd conductive layer.

[0006]

[Example]The 1st example of this invention is described according to drawing 1, drawing 2, and drawing 3 below. AA sectional view of drawing 1 and drawing 3 of the perspective view of the optical semiconductor device which requires drawing 1 for this example, and drawing 2 are the exploded perspective views of this optical semiconductor device. The insulating base 1 is acquired in these figures by laminating and calcinating the 1st, 2nd, and 3rd pedestal 2, 3, and 4 that comprises ceramics, respectively.

[0007]The surface layer 5 and the back layers 6, 7, and 8 which comprise nickel and gold are formed by plating etc. in near [where the rear face near the center of the surface and the rear face of the 1st pedestal 2 faces] the end. A through hole part is formed in four sides of the 1st pedestal 2, and the side layers 9, 10, 11, and 12 which change from nickel and gold to the surface are formed. The bore 13 is formed in the approximately center of the 2nd pedestal 3, the surface layer 14 which changes from nickel and gold to the surface is formed, and it is connected with the side layers 15 and 16. It is formed so that the side layers 17 and 18 may not connect with the surface layer 14 in the position which abbreviated-intersects perpendicularly with the side layers 15 and 16. The 3rd pedestal 4 is formed in approximately frame shape, and the side layers 19, 20, 21, and 22 which change from nickel and gold to the side are formed.

[0008]As mentioned above, as for the 1st conductive layer 23, the surface layer 5 near the center of the surface of the 1st pedestal 2, the side layers 10 and 12, and the back layer 6 near the center on the back are connected. The 2nd conductive layer 24 connects the surface layer 14 of the 2nd pedestal 3, the side layer 15 and the side layer 9 of the 1st pedestal 2, and the back layer 7. The 3rd conductive layer 25 connects the side layer 16 of the 2nd pedestal 3, the side layer 11 of the 1st pedestal 2, and the back layer 8. Thus, the 2nd and 3rd conductive layer 24 and 25 is formed near [where it connects with the surface layer 14 of the insulating base 1, and the rear face of the insulating base 1 faces] the end.

[0009]Installation adherence of OPTO semiconductor device 26 is carried out on the electroconductive glue 27 applied the surface [the 1st conductive layer 23], i.e., the center of the surface layer 5 neighborhood. OPTO semiconductor device 26 is a light emitting device which one side becomes from 200-400 micrometers, GaP which made ** at the time in the 250-300-micrometer-high abbreviated case, GsAsP, etc. Or OPTO semiconductor device 26 is a photo detector which one side makes the approximately rectangular parallelepiped shape 500-700 micrometers and whose height are 250-300 micrometers, and consists of a PIN photodiode formed in the P type board by diffusing phosphorus. In addition, as OPTO semiconductor device 26, a photo transistor etc. are applicable.

[0010]The metal thin wire 28 comprises gold etc. and is wired between the surface of OPTO semiconductor device 26 and the surface 14 of the 2nd conductive layer 24, i.e., a surface layer. The translucency resin 29 is formed so that an epoxy resin etc. may be comprised, and OPTO semiconductor device 26 and the metal thin wire 28 may be covered and the crevice of the surface of the insulating base 1 may be filled. The optical semiconductor device 30 is constituted by these parts.

[0011]Next, the case where this optical semiconductor device 30 is attached to the circuit board 31 is explained. The anode pattern 32 is formed on the circuit board 31 at the flat-surface abbreviation U shape so that it may be abbreviated-in agreement with the pitch of the 2nd and 3rd conductive layer 24 and 25 of the optical semiconductor device 30. The negative pole pattern 33 is formed in the approximately center of the anode pattern 32. when it attaches for Masakata, the 1st conductive layer 23 adheres to the negative pole pattern 33 -- the 2nd and 3rd conductive layer 24 and 25 -- the anode pattern 32 -- it has adhered on the 1st and 2nd placing part 34 and 35, respectively. Therefore, if the N type board of OPTO semiconductor device 26 is turned down and laid, operation of luminescence or light-receiving will be carried out.

[0012]And when this optical semiconductor device 30 is attached to an opposite direction.

similarly the 1st conductive layer 23 connects with the negative pole pattern 33. the 2nd and 3rd conductive layer 24 and 25 -- the anode pattern 32 -- it has adhered on the 2nd and 1st placing part 35 and 34, respectively. Therefore, forward voltage is impressed to OPTO semiconductor device 26, and luminescence or light-receiving is carried out. The representative circuit schematic of the optical semiconductor device concerning this example is explained according to drawing 4 (a) and (b). Drawing 4 (a) and (b) is a circuit diagram at the time of turning the N type board of OPTO semiconductor device 26, and a P type board down, and laying them, respectively. The side layers 10 and 12 which connect with the 1st conductive layer 23 are connected with the rear face of OPTO semiconductor device 26 in these figures. The side layer 9 linked to the 2nd conductive layer 24 is connected with the surface of OPTO semiconductor device 26 with the side layer 11 linked to the 3rd conductive layer 25.

[0013]Next, the 2nd example that can be manufactured easily is described according to the exploded perspective view of drawing 5 from an above-mentioned example. As for the 1st, 2nd, and 3rd pedestal 2A, 3A, and 4A of the optical semiconductor device 36 of this example, as compared with the 1st example, the side layers 12, 18, and 22 are not formed, respectively. Although the 1st conductive layer 23A has only the one side layer 10, when it attaches for Masakata or to an opposite direction, it adheres to the negative pole pattern 33. Therefore, when it attaches for Masakata or to an opposite direction, since the voltage of a normal direction is impressed by an OPTO semiconductor device, it operates normally.

[0014]Next, the 3rd example that can be manufactured still more easily is described according to the exploded perspective view of drawing 6 from the 2nd above-mentioned example. As for the 1st, 2nd, and 3rd pedestal 2B of the optical semiconductor device 37 of this example, and 3B and 4B, as compared with the 2nd example, the side layers 10, 17, and 20 are not formed, respectively. The through hole part 38 which the breakthrough was formed between the surface layer 5B formed in the surface of the 1st pedestal 2 and the back layer 6B formed near the center on the back, and flowed through the surface of the breakthrough in plating etc. is formed. When this optical semiconductor device 37 is attached for Masakata or to an opposite direction, the voltage of a direction with a normal OPTO semiconductor device is impressed.

[0015]The 4th example using two or more OPTO semiconductor devices is described according to the exploded perspective view of drawing 7. The 2nd conductive layer 24A connects each class 7, 9, 15C, 15E, 14D, and 19, The 3rd conductive layer 25A connects each class 8C, 11C, 16D, 16F, 14D, and 21C, the 2nd conductive layer 24B connects each class 7C, 9C, 15D, 14C, 15F, and 19C, and the 3rd conductive layer 25B connects each class 8, 11, 16C, and 21. The surface electrode of OPTO semiconductor devices 26 and 26C is wired by the 2nd conductive layer 24A and the 3rd conductive layer 25B, respectively.

[0016]As mentioned above, the 2nd conductive layer 24A and the 3rd conductive layer 25A faced in abbreviated point symmetry, and it was formed near the end, and they have connected mutually the center of the rear face of the insulating base 1C, and are wired with the surface electrode of OPTO semiconductor device 26 of the method of one. Similarly, the 2nd conductive layer 24B and the 3rd conductive layer 25A face the rear face of the insulating base 1C, are formed near the end, and are wired with OPTO semiconductor device 26C of another side.

[0017]Therefore, when it attaches for Masakata, the 2nd and 3rd conductive layer 24A and 25A is connected to the 1st and 2nd anode pattern on the circuit board, respectively, and the voltage of a normal direction is impressed to OPTO semiconductor device 26 of the method of one. Voltage is similarly built over OPTO semiconductor device 26C of another side. Next, when it attaches to an opposite direction, it is connected to the 2nd and 1st anode pattern, respectively, and the 2nd and 3rd conductive layer 24A and 25A requires the voltage of a normal direction for OPTO semiconductor device 26. OPTO semiconductor device 26C is also the same.

[0018]

[Effect of the Invention]Since this invention forms the 1st conductive layer near the center of the rear face of an insulating base like ****, also when this optical semiconductor device is attached to an opposite direction, the same polar voltage as the time of attaching for Masakata is impressed to the 1st conductive layer. And the 2nd and 3rd conductive layers are connected, and it faces and forms near the end of the rear face of an insulating base. Therefore, also when

it attaches to an opposite direction, the same polar voltage as the time of attaching for Masakata is impressed to the 2nd or 3rd conductive layer. Therefore, in attachment of for Masakata or an opposite direction, the voltage of a certain direction is impressed to the OPTO semiconductor device which it adheres to this 1st conductive layer, and is wired by the 2nd or 3rd conductive layer.

[0019]Therefore, since operation of luminescence or light-receiving is carried out when it attaches for Masakata or to an opposite direction, the impossible of operation by attaching to an opposite direction is cancelable. When attaching with an automatic machine, it is not necessary to recognize the directivity of an optical semiconductor device, and workability also becomes good.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a perspective view of the optical semiconductor device concerning the 1st example of this invention.
[Drawing 2]It is AA sectional view of drawing 1.
[Drawing 3]It is an exploded perspective view of the optical semiconductor device concerning the 1st example of this invention.
[Drawing 4]It is a representative circuit schematic of the optical semiconductor device concerning the 1st example of this invention. (a) and (b) show the case where turned the N type board of an OPTO semiconductor device, and the P type board down, and they are laid, respectively.
[Drawing 5]It is an exploded perspective view of the optical semiconductor device concerning the 2nd example of this invention.
[Drawing 6]It is an exploded perspective view of the optical semiconductor device concerning the 3rd example of this invention.
[Drawing 7]It is an exploded perspective view of the optical semiconductor device concerning the 4th example of this invention.
[Drawing 8]It is a sectional view of the conventional optical semiconductor device.
[Description of Notations]
1 Insulating base
23 23A The 1st conductive layer
24, 24A, and 24B The 2nd conductive layer
25, 25A, and 25B The 3rd conductive layer
26 26C OPTO semiconductor device

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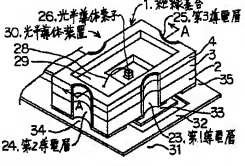
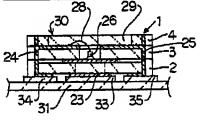
DRAWINGS

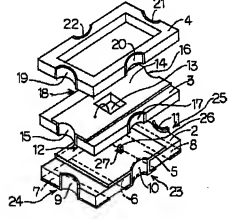
[Drawing 1]



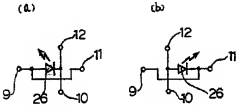
[Drawing 2]



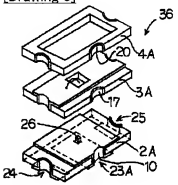
[Drawing 3]



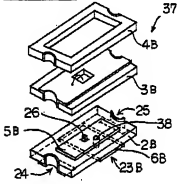
[Drawing 4]



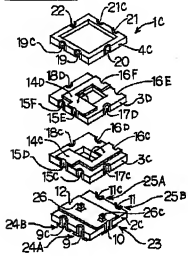
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Drawing 8]

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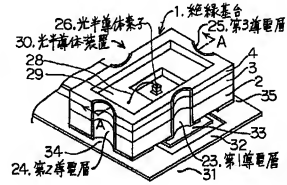
(54)【発明の名称】　光半導体装置

(57)【要約】
【目的】　逆方向に取付けても正常な動作を行なう光半導体装置を提供する。
【構成】　絶縁基台の表面の中央近傍と裏面の中央近傍に連なる第１導電層を設ける。絶縁基台の少なくとも裏面の相対する端部近傍に形成されかつ互いに接続された第２及び第３導電層を設ける。第１導電層の表面の中央近傍に固着されかつ第２又は第３導電層に配線された光半導体素子を設ける。



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【特許請求の範囲】

【請求項1】　絶縁基台の表面の中央近傍と裏面の中央近傍に連なって設けられた第1導電層と、前記絶縁基台の少なくとも裏面の相対する端部近傍に設けられかつ互いに接続された第2及び第3導電層と、前記第1導電層の表面の中央近傍に固着されかつ前記第2又は第3導電層に配線された光半導体素子とを具備した事を特徴とする光半導体装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は小型のチップ化された光半導体装置に関する。

【0002】

【従来の技術】近年チップ化された小型の略箱型形状をした光半導体装置が提案されている。これは例えば特開昭60－262476号公報の如く、図8の断面図にて示される。第1、第2配線層41と42は絶縁基台43の表面に位置し、側面を通り裏面に延びて形成されている。反射枠44が絶縁基台43上に積層されている。そして発光ダイオード45が第1配線層41上に固着され、第2配線層42に配線されている。

【0003】

【発明が解決しようとする課題】しかしてこの様な光半導体装置は例えば、第1、第2配線層41と42の裏面部がそれぞれ回路基板46の陽極、陰極パターン47と48上に位置する様に固着されて順電圧が印加されている。それ故、光半導体装置を間違がって逆方向に取付けた場合、すなわち第1、第2配線層41と42を陽極、陽極パターン48と47上に固着した場合、動作不能（発光しない）となる。故に本発明はかかる欠点を解消し、逆方向に取付けても正常な動作を行なう光半導体装置を提供するものである。

【0004】

【課題を解決するための手段】本発明は上述の課題を解決するために、絶縁基台の表面の中央近傍と裏面の中央近傍に連なって形成された第1導電層を設ける。そして絶縁基台の少なくとも裏面の相対する端部近傍に形成されかつ互いに接続された第2及び第3導電層を設ける。さらに第1導電層の表面の中央近傍に固着されかつ第2又は第3導電層に配線された光半導体素子を設ける。

【0005】

【作用】上述の如く本発明は第1導電層を絶縁基台の裏面の中央近傍に形成するので、この光半導体装置を正方向に又は逆方向に取付けた時、第1導電層に同一極性の電圧が印加される。そして第2及び第3導電層を接続して絶縁基台の裏面の端部近傍に相対して形成する。故に正方向に又は逆方向に取付けた時、第2又は第3導電層に同一極性の電圧が印加される。

【0006】

【実施例】以下に本発明の第1実施例を図1、図2、図3に従って説明する。図1は本実施例に係る光半導体装置の斜視図、図2は図1のAA断面図、図3は本光半導体装置の分解斜視図である。これらの図に於て、絶縁基台1は例えばそれぞれセラミックから成る第1、第2、第3基台2、3、4を積層して焼成する事により得られたものである。

2

【0007】第1基台2の表面と裏面の中央近傍と裏面の相対する端部近傍に於て、ニッケルと金から成る表面層5と裏面層6、7、8がメッキ等により形成されている。第1基台2の4つの側面に於てスルーホール部が形成され、その表面にニッケルと金から成る側面層9、10、11、12が形成されている。第2基台3の略中央に透孔13が形成され、表面にニッケルと金から成る表面層14が形成され、側面層15、16と接続されている。側面層17、18が側面層15、16と略直交する位置に於てかつ表面層14と接続しない様に形成されている。第3基台4は略額縁状に形成され、その側面にニッケルと金から成る側面層19、20、21、22が形成されている。

【0008】上述の様に、第1導電層23は第1基台2の表面の中央近傍の表面層5と側面層10、12と裏面の中央近傍の裏面層6を接続されたものである。第2導電層24は第2基台3の表面層14、側面層15と第1基台2の側面層9、裏面層7を接続したものである。第3導電層25は第2基台3の側面層16と第1基台2の側面層11、裏面層8を接続したものである。この様に、第2、第3導電層24、25は絶縁基台1の表面層14に接続しかつ絶縁基台1の裏面の相対する端部近傍に形成されたものである。

【0009】光半導体素子26は第1導電層23の表面すなわち表面層5の中央近傍に塗布された導電性接着剤27上に載置固着されている。光半導体素子26は例えば1辺が200～400μm、高さが250～300μmの略ないころ状をなしたGaP、GsAsP等からなる発光素子である。または光半導体素子26は例えば1辺が500～700μm、高さが250～300μmの略直方体状をなし、P型基板に撰を拡散して形成されたPINフォトダイオードからなる受光素子である。その他に光半導体素子26として、フォトトランジスター等も適用できる。

【0010】金属細線28は金等から成り、光半導体素子26の表面と第2導電層24の表面、すなわち表面層14との間に配線されている。透光性樹脂29はエポキシ樹脂等から成り、光半導体素子26と金属細線28を覆ってかつ絶縁基台1の表面の凹部を埋める様に形成されている。これらの部品により光半導体装置30が構成されている。

【0011】次にこの光半導体装置30を回路基板31に取付けた場合を説明する。陽極パターン32は光半導体装置30の第2、第3導電層24、25のピッチと略

一致する様に、回路基板３１上に平面略コ字状に形成されている。陰極パターン３３は陽極パターン３２の略中央に形成されている。正方向に取付けた場合、第１導電層２３は陰極パターン３３に固着され、第２、第３導電層２４、２５が陽極パターン３２のそれぞれ第１、第２載置部３４、３５上に固着されている。従って光半導体素子２６のN型基板を下にして載置していれば、発光又は受光の動作をする。

【００１２】そしてこの光半導体装置３０を逆方向に取付けた場合、第１導電層２３は同じく陰極パターン３３と接続する。第２、第３導電層２４、２５が陽極パターン３２のそれぞれ第２、第１載置部３５、３４上に固着されている。従って光半導体素子２６に順電圧が印加され発光又は受光をする。更に本実施例に係る光半導体装置の等価回路図を図４（ａ）、（ｂ）に従って説明する。図４（ａ）、（ｂ）はそれぞれ光半導体素子２６のN型基板、P型基板を下にして載置した場合の回路図である。これらの図に於て、第１導電層２３と共に接続する側面層１０、１２は光半導体素子２６の裏面と接続している。第２導電層２４と接続する側面層９は第３導電層２５と接続する側面層１１と共に光半導体素子２６の表面と接続している。

【００１３】次に上述の実施例より簡単に製作できる第２実施例を図５の分解斜視図に従って説明する。第１実施例と比較して本実施例の光半導体装置３６の第１、第２、第３基台２Ａ、３Ａ、４Ａはそれぞれ側面層１２、１８、２２が形成されていない。第１導電層２３Ａは１つの側面層１０しか有していないが、正方向又は逆方向に取付けた場合、陰極パターン３３に固着される。故に正方向に又は逆方向に取付けた場合、光半導体素子には正常な方向の電圧が印加するので正常に動作する。

【００１４】次に、上述の第２実施例より更に簡単に製作できる第３実施例を図６の分解斜視図に従って説明する。第２実施例と比較して、本実施例の光半導体装置３７の第１、第２、第３基台２Ｂ、３Ｂ、４Ｂはそれぞれ側面層１０、１７、２０が形成されていない。第１基台２の表面に形成された表面層５Ｂと裏面の中央近傍に形成された裏面層６Ｂとの間に、貫通孔が形成されその貫通孔の表面をメッキ等で導通されたスルーホール部３８が形成されている。この光半導体装置３７を正方向に又は逆方向に取付けた場合、光半導体素子は正常な方向の電圧が印加される。

【００１５】更に、複数の光半導体素子を用いた第４実施例を図７の分解斜視図に従って説明する。第２導電層２４Ａは各層７、９、１５Ｃ、１５Ｅ、１４Ｄ、１９を接続し、第３導電層２５Ａは各層８Ｃ、１１Ｃ、１６Ｄ、１６Ｆ、１４Ｄ、２１Ｃを接続し、第２導電層２４Ｂは各層７Ｃ、９Ｃ、１５Ｄ、１４Ｃ、１５Ｆ、１９Ｃを接続し、第３導電層２５Ｂは各層８、１１、１６Ｃ、２１を接続したものである。光半導体素子２６、２６Ｃ

の表面電極はそれぞれ第２導電層２４Ａと第３導電層２５Ｂに配線されている。

【００１６】上述の様に、第２導電層２４Ａと第３導電層２５Ａは絶縁基台１Ｃの裏面の中心を略点対称的に相対しかつ端部近傍に形成されかつ互いに接続しており、１方の光半導体素子２６の表面電極と配線されている。同様に第２導電層２４Ｂと第３導電層２５Ａは絶縁基台１Ｃの裏面に相対して端部近傍に形成され、他方の光半導体素子２６Ｃと配線されている。

【００１７】従って正方向に取付けた場合、第２、第３導電層２４Ａ、２５Ａはそれぞれ回路基板上の第１、第２陽極パターンに接続され１方の光半導体素子２６に正常な方向の電圧が印加される。同様に他方の光半導体素子２６Ｃにも電圧がかかる。次に逆方向に取付けた場合、第２、第３導電層２４Ａ、２５Ａはそれぞれ第２、第１の陽極パターンに接続され、光半導体素子２６に正常方向の電圧がかかる。光半導体素子２６Ｃも同様である。

【００１８】

【発明の効果】本発明は上述の如く、第１導電層を絶縁基台の裏面の中央近傍に形成するのでこの光半導体装置を逆方向に取付けた場合も第１導電層には正方向に取付けた時と同一極性の電圧が印加される。そして第２及び第３導電層を接続して絶縁基台の裏面の端部近傍に相対して形成する。故に逆方向に取付けた場合も、第２又は第３導電層には正方向に取付けた時と同一極性の電圧が印加される。従ってこの第１導電層に固着され第２又は第３導電層に配線される光半導体素子には、正方向又は逆方向の取付の場合、一定方向の電圧が印加される。

【００１９】従って正方向に又は逆方向に取付けた場合、発光又は受光の動作をするので、逆方向に取付ける事による動作不能を解消できる。また自動機で取付ける場合、光半導体装置の方向性を斟酌する必要がなく作業性も良くなる。

【図面の簡単な説明】

【図１】本発明の第１実施例に係る光半導体装置の斜視図である。

【図２】図１のＡＡ断面図である。

【図３】本発明の第１実施例に係る光半導体装置の分解斜視図である。

【図４】本発明の第１実施例に係る光半導体装置の等価回路図である。（ａ）、（ｂ）はそれぞれ光半導体素子のN型基板、P型基板を下にして載置した場合を示す。

【図５】本発明の第２実施例に係る光半導体装置の分解斜視図である。

【図６】本発明の第３実施例に係る光半導体装置の分解斜視図である。

【図７】本発明の第４実施例に係る光半導体装置の分解斜視図である。

【図８】従来の光半導体装置の断面図である。

5

【符号の説明】

1　絶縁基台

23、23A　第1導電層

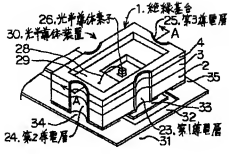
6

24、24A、24B　第2導電層

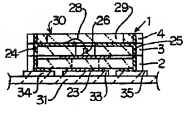
25、25A、25B　第3導電層

26、26C　光半導体素子

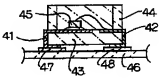
【図1】



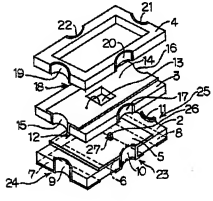
【図2】



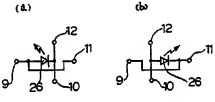
【図8】



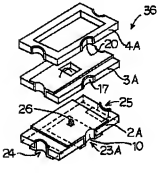
【図3】



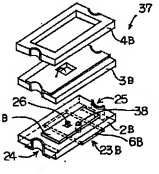
【図4】



【図5】



【図6】



【図7】